CLAIMS

What is claimed is:

1. A system for detecting and correcting errors in a data structure, comprising:

a data structure stored in a plurality of memory devices associated with a memory address;

a data separator that partitions the data structure into adjacent bit pair domains, such that a single adjacent bit pair from each of the plurality of memory devices is assigned to an adjacent bit pair domain; and

an error detection and correction (EDC) component that detects and corrects errors associated with a given adjacent bit pair domain.

2. The system of claim 1, the EDC component detects and corrects errors associated with the plurality of adjacent bit pair domains in a sequential manner.

3. The system of claim 1, further comprising at least one additional EDC component, such that errors associated with the plurality of adjacent bit pair domains are detected and corrected by a respective EDC component in a parallel manner.

4. The system of claim 1, the data separator being a buffer/multiplexer device coupled between the plurality of memory devices and the EDC component.

5. The system of claim 4, the buffer/multiplexer is coupled to the plurality of memory devices through a data bus and to the EDC component through a mid-bus, the buffer/multiplexer receives the data structure from the plurality of memory devices and transmits the adjacent bit pair domains in a sequential manner over the mid-bus to the EDC component.

6. The system of claim 1, the data structure comprising B bits and the plurality of adjacent bit pair domains having B/2 bits, where B is an integer multiple of four that is greater than or equal to eight.

7. The system of claim 6, the data structure comprising 288 bits and each of the plurality of adjacent bit pair domains having 144 bits.

8. The system of claim 1, the data structure having K * W bits, where K is the number of the plurality of memory devices forming the system memory, and W is the column widths of the plurality of memory devices.

9. The system of claim 1, further comprising a check bit generator that generates check bits that are aggregated with data bits to form an adjacent bit pair domain, the adjacent bit pair domains being combined to form the data structure.

10. A server comprising the system of claim 1.

11. The system of claim 1 enabling chipkill functionality for the plurality of memory devices.

12. A memory system comprising:

a plurality of memory devices operative to store a data structure over the plurality of memory devices corresponding to a given memory address;

a buffer/multiplexer device that transmits and receives the data structures over a first bus and transmits and receives adjacent bit pair domain data over a second bus;

the adjacent bit pair domain data comprising data bits and check bits assigned to a given adjacent bit pair domain, such that a single adjacent bit pair from each of the plurality of memory devices corresponding to the given memory address is assigned to a given adjacent bit pair domain for each of a plurality of adjacent bit pair domains; and

a controller operative to transmit and receive adjacent bit pair domain data over the second bus and operative to transmit and receive data blocks corresponding to the adjacent bit pair domain data over a third bus.

13. The system of claim 12, the controller being one of a memory controller and a cache coherency controller.

14. The system of claim 12, the controller further comprising an error detection and correction (EDC) component operative to detect and correct single bit errors and adjacent double bit errors associated with a respective adjacent bit pair domain.

15. The system of claim 14, the controller further comprising a check bit generator that generates check bits associated with respective adjacent bit pair domains, the check bits being employed by the EDC component to correct single bit errors and adjacent double bit errors.

16. An error correction system, comprising:

means for partitioning a data structure into a plurality of adjacent bit pair domains, each adjacent bit pair domain being populated with a single adjacent bit pair from each of a plurality of memory devices associated with a given memory address; and

means for detecting and correcting single bit errors and adjacent double bit errors associated with a respective adjacent bit pair domain.

17. The system of claim 16, further comprising means for transmitting the plurality of adjacent bit pair domains in a sequential manner to the means for detecting and correcting.

18. The system of claim 16, the means for detecting and correcting comprising a plurality of means for detecting and correcting single bit errors and adjacent double bit errors associated with different respective adjacent bit pair domains.

19. A method of reading data from a plurality of memory device defining a system memory, the method comprising:

reading a data structure from rows of the plurality of memory devices associated with a given memory address;

separating the data structure into a plurality of adjacent bit pair domains, each adjacent bit pair domains having a single adjacent bit pair from each of the plurality of memory devices associated with the given memory address; and

performing error detection and correction on the plurality of adjacent bit pair domains.

20. The method of claim 19, the performing error detection and correction on the plurality of adjacent bit pair domains comprising performing error detection and correction on the respective adjacent bit pair domains in one of a sequential and parallel manner.

21. The method of claim 19, the performing error detection and correction on the plurality of adjacent bit pair domains comprising performing error detection and correction to correct for single bit errors and adjacent double bit errors in respective adjacent bit pair domains.

22. The method of claim 19, further comprising discarding check bits associated with corrected respective adjacent bit pair domains, and combining the corrected respective adjacent bit pair domains to form a data block.

23. A method of storing data into a plurality of memory device defining a system memory, the method comprising:

receiving a data block for storage;

assigning adjacent data bit pairs to respective adjacent bit pair domains, each adjacent bit pair domain having a single adjacent bit pair associated with each of a plurality of memory devices for a given memory address;

generating check bits for each adjacent bit pair domain;

populating each respective adjacent bit pair domain with its associated check bits;

combining the adjacent bit pair domains to provide a data structure for storage; and

writing the data structure into the plurality of memory devices at the given memory address.

24. The method of claim 23, the generating and aggregation of check bits being performed in one of a sequential manner and a parallel manner.